REMARKS

Claims 1-6, 13-18, and 24-29 are pending in this application. Claims 7-12, 19-23, and 30-34 have been withdrawn as a non-elected species for prosecution. The Examiner has rejected claims 1-6, 13-18, and 24-29. The Examiner has also raised other issues with respect to the application that the applicants will now address.

In the Drawings

The Examiner raised various objections with respect to the drawings and lack of proper reference numbers in the drawings. Accordingly, the applicants have corrected these problems by amending Figs. 1,2,3,4,10,19, and 20, as indicated in red thereon. Applicants assume that this resolves the issues raised with respect to the drawings.

In the Specification

The Examiner noted some apparently incorrect numbers as well as a misspelled word. Applicants have accordingly corrected these deficiencies. Applicants now presume that all of these deficiencies have been resolved.

Claim Objections

The Examiner suggested the addition of the word "paths" in line 6, claim 1, between "mounting" and "arrays" to avoid confusion and aid consistency to the language. Accordingly, the Applicants have made the recommended amendment.

Claim rejections 35 USC § 112

The Examiner raised four different rejections with respect to claims 1, 2, 13, and

24 under 35 USC § 112.

One of the rejections relates to claim 2, and the Applicants, as suggested by the Examiner, have amended the claim by deleting the word "leads" in line 3 and replacing it with "Connection Elements" to be consistent with claim 1.

The other three rejections relate to claims 1, 13, and 24 wherein it noted that they each refer to either "carrier interface", or "interface coupled". It was noted there was some confusion with this term. First it is noted that the term "carrier interface" is identified at the end of the paragraph starting at line 20 on page 8. Additionally, to help clarify this term, the Applicants have accordingly corrected the application to more clearly delineate what the term "carrier interface" means. Such correction has been added to the end of the paragraph starting on Page 8, line 20. It is noted that the key additional language inserted therein, regarding connective links between the mounting pads on either side of the carrier is taken from the claims as originally filed with the application, (See original, claim 2), etc. Accordingly, there has been no new matter added in making this adjustment to the application. Fig. 1 has also been amended to better show the same.

Claims rejections under 35 USC §102 and § 103

Rejection of claim 1 under 35 USC §102b as being anticipated by Coller et al. (U.S. Patent No. 4,696,525)

It was specifically noted by Examiner in this rejection:

> Regarding claim 1, Coller teaches an electronic circuit module comprising: of at least one IC package unit, each unit having a carrier (Reference Number 30) having first and second IC package mounting locations (Reference Numbers 50 and 52, respectively) on opposed sided thereof, said first mounting location (Reference Number 50) having a first mounting pad array (Reference Number

78) said second mounting location (Reference Number 52) having a second mounting pad array (Reference Number 86), said first and second mounting arrays being coupled to a carrier interface; and a pair of IC packages (Reference Numbers 100A and 100B), each package having a package body (Reference Number 104) containing an integrated circuit chip and a plurality of connection elements (Reference Number 112) coupled to said chip and extending at least to the surface of the said body, the connection elements of said first package being conductively bonded to said first mounting pad array (See Figure 3), the connection elements of said second package being conductively bonded to said second mounting pad array (See figure 3); and a printed circuit board (Reference Number 130) having at least one interconnection pad array (Reference Number 134) affixed thereto, each interconnection pad array coupled to circuitry (Reference Number 132) on the printed circuit board and conductively bonded to the interface of a single IC package unit (See figure 3).

Applicants note that the so called mounting pad arrays of the type disclosed in Coller are totally different than those disclosed, depicted, as well as claimed in Applicants' invention. Coller, in fact does not have mounting pad arrays but rather employees a double-pronged lead 62 with a first prong 86 and a second78 (See Fig 2, and Fig. 3). This double-pronged lead extends out of the carrier body 56, with the one prong designated 78 bent upward, and one prong designated 86 bent downward. Each prong of the leads 78 and 86 form a set or array in the form of a nest. Accordingly, an integrated circuit package 100A or 100B is then inserted into the pronged arrays, or nests, thereby created. Thus, the leads 62 with prongs 78 and 86 are totally dissimilar from the pads of the Applicants' invention on which the IC packages are mounted in Applicants' arrangement. In fact, as stated in claim 1, lines 3-6 of Applicants' application, as well as depicted in the drawings, the mounting locations with the first and second mounting pad arrays are on either side of the carrier as depicted in the various figures. For instance, in Fig. 1, one set of mounting pad arrays is 103 on the top of carrier 101. Additionally, even in the one example, in a variation of the Applicant's invention, in which the carrier, 2102, (Fig. 21), has leads 2108, the pads, and 2105A are on the top surface and bottom surface of the carrier.

Accordingly, applicants respectfully traverse the Examiner's rejection and note

that it would be impossible to practice the invention of Coller with the Applicant's invention. Applicants' invention has opposing sets of pads on either side of the carrier. On the other hand, Coller does not have pad arrays, but rather a double-pronged lead, the leads of which are bent to form two nests to at least frictionally hold an integrated circuit package.

Rejection of claims 13, 14, 15, and 17 under 35 USC §102(b) as being anticipated by Coller et al.

Applicants again note that the same differences exist with respect to independent claim 13 and its dependant claims as is noted with respect to claim 1. Coller provides a unique bent, two-pronged lead that creates, in fact, a type of gripping mechanism formed into a nest that can hold an integrated circuit chip. On the other hand, the applicants' have mounting pad arrays, located on either side of the carrier. Thus, as noted above it would be impossible to practice the applicants' invention with Coller's invention as they teach away from each other.

Rejection of claims 4, 16, 18, 27, and 29 under 35 USC § 103(a) as being unpatentable over Coller et al. in view of Levy et al. (U.S. Patent Number 5,867,353).

Applicants' reassert the arguments raised with respect to the 102 rejections as noted above, and reiterate that Coller, in fact, teaches a totally different method that would be impossible to practice with the applicants' invention. Consequently, it is arguable as to whether or not Coller and Levy can be combined and even if they can the result would be significantly different.

Conclusion

Claims 1-6, 13-18, and 24-29 are all pending in this application. Applicants thank

the Examiner for his consideration in reviewing this application and suggesting various corrections to a number of problems cited. Based upon the arguments made above, and the corrections made to the application the applicants' respectfully request that the Examiner reconsider the rejection of the claims, and allow them.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE TO ORIGINAL APPLICATION

Deletions are in **bold** and setoff by brackets **[ ]** and additions are in **bolded italics.**

In the specification:

The paragraph starting on page 8 line 20 was amended as follows:

The present invention provides for an improved multi-chip module having increased chip density over conventional modules presently in use. All embodiments of the improved module include a circuit board having an array of electrical interconnection pads to which are mounted a plurality of IC package units. Each IC package unit includes a package carrier having multiple IC packages, which are mounted on opposite sides of the package carrier. The package units may be mounted on one or both sides of the circuit board. The connection elements (leads or pads) of each of the packages are coupled to a carrier interface, which may or may not include discrete carrier leads. **The**

carrier interface includes conductive links 111 between the mounting pads 103 on opposite sides of the package carrier within the package carrier as indicated with two examples in Fig. 1. Naturally, each set of opposing pads would be connected within carrier 101 in some similar fashion.

The paragraph starting on page 9 at line 10 was amended as follows:

Referring now to Figure 3, multiple first embodiment package units 201 (in this example, four) are shown ready for mounting on a circuit board 301. In this example, two package units 201A and 201B will be mounted on the upper surface 302U of the circuit board 301, while two package units 201C and 201D will be mounted on the lower surface 302L thereof. One IC package 105H of each package unit 201 fits within its own recess 303 in the circuit board 301 so that it is **[comletely]** **completely** hidden from view, while the other IC package 105E is completely exposed. The surrounding edges of each recess are equipped with a set of board electrical connection contact pads 304. The leads of each hidden package 105H will make direct contact with the contact pads of its recess and will be routed within the circuit board 301 to the appropriate interconnection sites. The leads 104 of the exposed IC package 105E are coupled to the leads 104 of the connections which penetrate the laminar carrier 101. By using a multi-conductive-layer carrier, rerouting of the lead positions may be accomplished. For example hidden package 105H by means of, if both packages are identical memory chips requiring individual chip select signals, a chip select signal may be routed to an unused lead of the hidden IC package 105H, then routed within the carrier 101 to the proper location on the exposed IC package 105E. As all other signals may be shared in common, interconnections between leads of the hidden IC package 105H and identically corresponding leads of the exposed IC package 105E may be made by plated through-holes in the carrier 101. The circuit board 301 may incorporate one or more heat-sink layers **[304]** **305** with which the bodies of hidden IC packages **[104H]** **105H** are in surface-to-surface contact, either directly or indirectly via a thin layer

of thermally-conductive paste, such as zinc oxide paste (not shown).

The paragraph starting on page 10 line 9 was amended as follows:

Referring now to Figure 4, surface mounting of the package units 201 on the circuit board 301 has resulted in a completed first embodiment module 401. A cross sectional view through the plane ABCD 402 provides the view of Figure 5. **As is well known in the art and schematically shown in Fig. 5 an integrated circuit chip 107 is typically imbedded in a carrier body 106.**

In the claims:

Claims 1 and 2 as follows:

1. An electronic circuit module comprising:

at least one IC package unit, each unit having

a carrier having first and second IC package mounting locations on opposed sided thereof, said first mounting location having a first mounting pad array, said second mounting location having a second mounting pad array, said first and second mounting **pad** arrays being coupled to a carrier interface; and

a pair of IC packages, each package having a package body containing an integrated circuit chip and a plurality of connection elements coupled to said chip and extending at least to the surface of said body, the connection elements of said first package being conductively bonded to said first mounting pad array, the connection elements of said second package being conductively bonded to said second mounting pad array; and

a printed circuit board having at least one interconnection pad array affixed thereto, each interconnection pad array coupled to circuitry on the printed circuit board and conductively bonded to the interface of a single IC package unit.

2. The electronic circuit module of claim 1, wherein individual mounting pads of said first mounting pad array are coupled to individual mounting pads of said second mounting pad array by means of conductive links within the carrier, and the **[leads]** **connection elements** of one of said IC packages are conductively bonded directly to said interconnection pad array.